A Highly Efficient Linearized Wide-Band CDMA Handset Power Amplifier Based on Predistortion Under Various Bias Conditions

Gary Hau, *Member, IEEE*, Takeshi B. Nishimura, *Member, IEEE*, and Naotaka Iwata, *Senior Member, IEEE*

***Abstract*—This paper investigates the use of amplifier linearization for performance improvement on a power amplifier developed for a wide-band CDMA (W-CDMA) system. Predistortion technique was chosen due to its compact size, which is suitable to implement in handsets. A predistorter (PD) monolithic-microwave integrated-circuit based on a heterojunction FET (HJFET) was designed and fabricated. Depending on the control voltage, the PD achieves both gain expansion and compression characteristics, which is shown to be important for compensating various amplifier nonlinearities. The power performances of an HJFET amplifier with and without a PD are compared. Due to the variation of the amplifier's responses under high and low quiescent current levels, the PD response required for optimum distortion cancellation in each case is examined. The linearized amplifier demonstrates a state-of-the-art power-added efficiency (PAE) of 57.4% under W-CDMA criteria, resulting from a 5-dB reduction in adjacent channel leakage power ratio. In addition, the use of power control in a W-CDMA system requires amplifiers with good efficiency over a wide range of output power. By combining a bias control scheme with predistortion, it is shown that a high PAE of over 40% can also be achieved for a 20-dB output power range. The improvements achieved are attributed to the alleviation of amplifier's nonlinearities after linearization.**

***Index Terms*—FET, linear power amplifier, linearization, microwave amplifier, predistortion.**

I. Introduction

WIRELESS communication systems have experienced phenomenal growth in recent years. In order to accommodate high data-rate transmission as well as Internet access, extensive research has been done on a third-generation network such as a wide-band CDMA (W-CDMA) system [1]. A W-CDMA system employs a spectrally efficient modulation scheme, hybrid phase-shift keying (HPSK), which poses a stringent requirement on the linearity of handset power amplifiers in order to minimize spectral regrowth and maintain modulation accuracy. In addition, since power amplifiers consume a significant amount of battery power, high power-added efficiency (PAE) is preferred for maximizing standby and talk time of handsets, which are important design concerns.

Conventional class-A- or class-AB-biased amplifiers typically operate at a certain degree of power backoff to satisfy the low distortion specification. The attendant disadvantage is that the PAE drops when an amplifier operates at less than saturation power [2]. With the view of the efficiency–linearity requirement, common design practice also focuses on improving input and output matching networks of power amplifiers to obtain optimum performance [3], [4]. Although improvements have been reported, the inherent tradeoffs between efficiency and linearity remain unresolved.

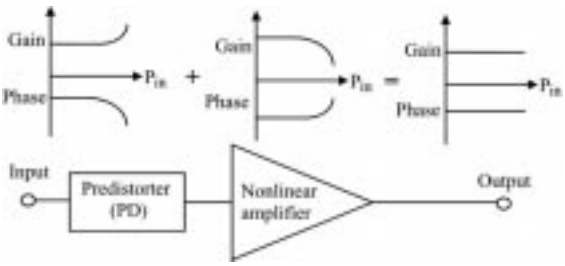

Fig. 1. Principle of predistortion linearization.

One solution to achieve the seemingly conflicted goals is to employ linearization techniques. By reducing the distortion level at the output of amplifiers by means of external circuitry, less power backoff is required and, thus, improves the efficiency of operation. Such techniques have received considerable attention recently and extensive research has been done in this area with applications varied from wireless handsets and basestations to satellite systems [5], [6]. The most commonly used techniques include feed-forward, feedback, and predistortion. Feed-forward linearization offers the most superior distortion improvement, but has the disadvantages of requiring extra error amplifier and bulky size, limiting it to basestation application [7], [8]. The conventional feedback technique suffers the drawback of gain loss of a similar degree to distortion improvement [9], as well as stability concern [10]. Predistortion linearization usually provides moderate distortion improvement [11], [12] at little extra cost and impact on output power. It also has the advantages over other techniques in terms of miniaturized size, low complexity, and stable operation, making it attractive for handset application.

Fig. 1 shows a block diagram of predistortion linearization. The predistorter (PD) has transfer characteristics inverse to that of the nonlinear amplifier. The nonlinear gain compression of the amplifier is compensated by the expansion characteristic of the PD. A similar effect applies to the phase nonlinearity. In principle, linear gain and phase are obtained at the output, achieving distortion-free signal amplification. Recent develop-

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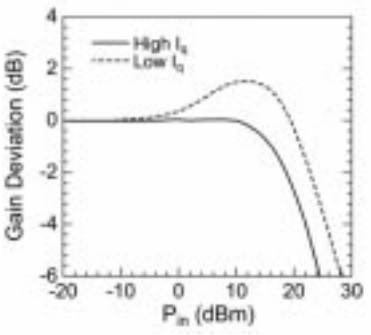


Fig. 2. Typical gain deviation characteristics of an amplifier under different I_q [3].

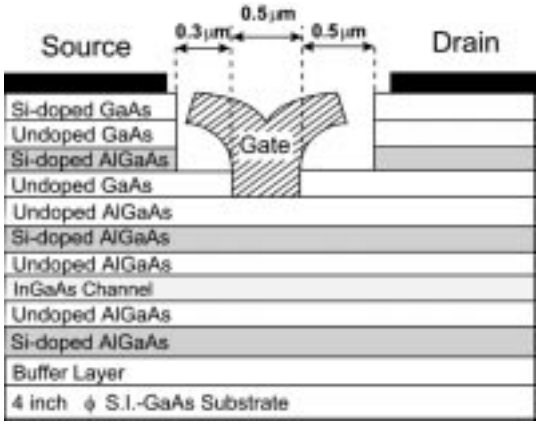


Fig. 3. Cross section of the developed double-doped AlGaAs/InGaAs/AlGaAs HJFET.

ment on the PD has focused on lower current operation and simple circuit configuration aimed for wireless and satellite applications [13]–[16]. These PDs employed either an FET [13], [14] or a diode [15], [16] as the nonlinearity generator, and successfully compensated nonlinearities of amplifiers at various frequency bands with distortion reduction ranged from 5 to 10 dB. However, high insertion loss (IL) of 5 dB to over 20 dB were reported on these PDs that require extra buffer amplifiers to bring up the predistorted signal level and are, therefore, unsuitable for handset application.

PD design usually emphasizes linearizing amplifiers with a gain compression characteristic [13]–[16]. However, amplifiers biased at low quiescent current (I_q) show different gain responses [3]. Fig. 2 compares the typical gain deviation characteristics of an amplifier operated at different level of I_q. It can be seen that the gain for the low I_q case (less than 1% of maximum drain current, I_{max}) expands slightly before compression occurs, whereas the gain compresses gradually as the input power level increases for the high I_q operation (over 2.5% I_{max}) [3]. The effect of the gain expansion on the choice of the response of the PD has not been investigated. In addition, prior designs have concentrated on applying PDs to linearize amplifiers under fixed-bias condition [13]–[16]. In wireless systems, such as W-CDMA, which realize power control, dynamic bias control would be applied to handset amplifiers for efficiency improvement at low-power operation, and the viability of the PD for compensating nonlinearities at different bias levels will become critical.

To address these issues, this paper presents a detailed study on the design and performance of a linearized power amplifier based on the predistortion technique. The circuit was designed to investigate its suitability for W-CDMA handset application. First, the heterojunction FET (HJFET) employed in this work is illustrated. The design of a PD is then detailed with emphasis on considerations such as low loss and small size. Measured characteristics of the PD monolithic microwave integrated circuit (MMIC) are shown with discussion on its versatile gain deviation characteristics. Next, several measured results, comparing the performance of an amplifier with and without a PD, are presented. The effect on the choice of the PD characteristic due to the variation on the amplifier's gain response under different I_q operation is studied, and a few tradeoffs on operation are discussed. Finally, the impact of combining the PD and bias control on the low-output power performance of the amplifier is examined.

II. HJFET

The device used in this work for the PD and amplifier was a double-doped AlGaAs/InGaAs/AlGaAs HJFET [3], and its cross section is shown in Fig. 3. It has a recess structure with a source-to-gate recess spacing of 0.3 μm, a gate length of 0.5 μm and a gate-to-drain recess spacing of 0.5 μm. The active part of the FET consists of an undoped $In_{0.2}Ga_{0.8}As$ channel layer sandwiched between Si-doped $Al_{0.22}Ga_{0.78}As$ layers. An undoped $Al_{0.22}Ga_{0.78}As$ Schottky layer was incorporated on the upper Si-doped $Al_{0.22}Ga_{0.78}As$ layer to achieve a high gate-to-drain breakdown voltage (BV_{gd}) [17]. A double-recess structure was fabricated by electron cyclotron resonance plasma dry-etching with SF_6 and BCl_3 gases using the $Al_{0.22}Ga_{0.78}As$ layer as an etch stop [18]. The resulting standard deviation of the threshold voltage was less than 20 mV on a 4-in wafer. WSi metal was sputter deposited onto the narrow recess to form the 0.5-μm-long gate. A multilayer cap structure was employed to reduce on resistance (R_{on}) [19].

The I_{max} of the fabricated HJFET, measured at a gate-to-source voltage (V_{gs}) of 1.5 V is 570 mA/mm. A maximum transconductance of 300 mS/mm is achieved at around V_{gs} equal to 0 V. The BV_{gd} is 18 V measured at a gate current density of 1 mA/mm. The HJFET shows an R_{on} of 1.7 $\Omega \cdot$ mm. This low R_{on} is essential for high PAE under low-voltage operation. Detailed power performance of the device can be found elsewhere [20].

III. PD

A. Basic Operation

The schematic diagram of a miniaturized PD is shown in Fig. 4. The PD employs an HJFET as the nonlinear element, and was designed to linearize an amplifier with gain compression and positive phase deviation [3]. The HJFET is arranged like a switch, which acts as a variable resistor, where the drain (D) and source (S) are connected to ground through inductors L, and the gate (G) is connected to ground via capacitor C. Two

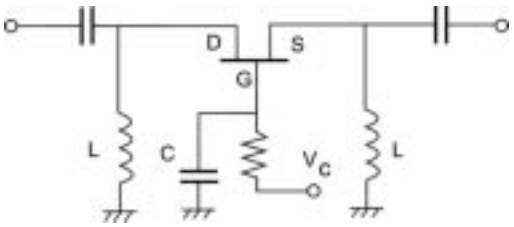
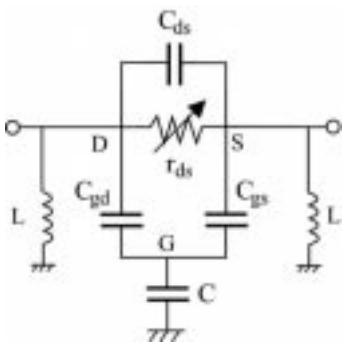


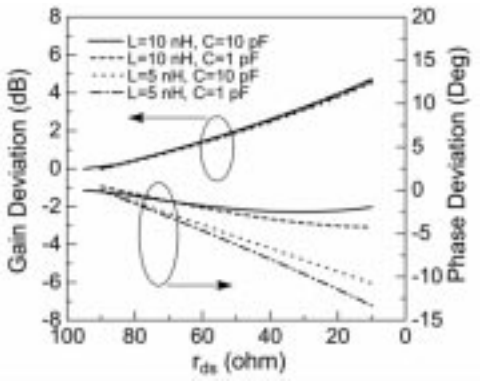
Fig. 4. Schematic of the PD. The HJFET is arranged like a switch and used as a nonlinearity generator.

capacitors are employed at the input and output of the PD for dc blocking and matching purposes. A bias control voltage (V_c) is applied to the gate of the PD through a bias resistor. The characteristic of the PD is determined by the drain-to-source resistance (r_{ds}) of the HJFET, which is a function of V_c. To obtain gain expansion operation, r_{ds} should decrease with increasing input power [15]. It has been previously reported that such a condition can be achieved when the HJFET is biased near pinchoff [21]. Inductors L are included for attaining negative phase deviation on the PD.

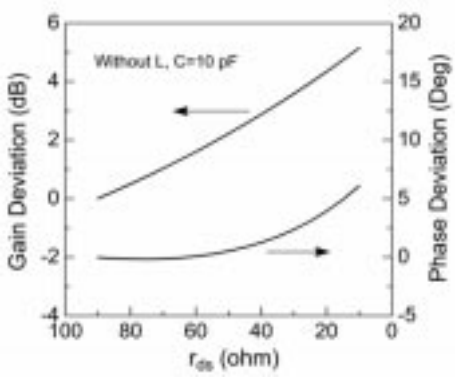
Fig. 5(a) shows a simplified equivalent-circuit model of the PD biased near pinchoff [22] for estimating the performance. The drain-to-source, gate-to-drain, and gate-to-source capacitances (C_{ds}, C_{gd}, and C_{gs}, respectively) were assumed to be constant because the variations were negligible compared with the variation of r_{ds} as a function of input power. The capacitance values were obtained from a large-signal HJFET model [23]. Fig. 5(b) shows the simulated responses of the PD for different values of L and C as a function of r_{ds}. Gain expansion and negative phase deviation are achieved with decreasing r_{ds}. It can be seen that, by reducing the values of L and C, the degree of negative phase deviation increases without affecting the gain expansion level. Thus, L and C can be optimized to fit the phase characteristic of an amplifier to be linearized. Fig. 5(c) shows the simulated responses of the PD without inductors L, whereas the capacitor C was set equal to 10 pF. Although gain expansion is also achieved, a positive phase deviation is observed, which demonstrates the function of inductors L on the phase response of the PD. This type of PD can be applied for linearizing amplifiers with a negative phase characteristic [14].



(a)



(b)



(c)

Fig. 5. (a) Equivalent circuit of the PD. Simulated responses of the PD: (b) with inductors L and (c) without inductors L as a function of r_{ds}.

B. Measured Performance

The PD was fabricated based on an HJFET with a gatewidth (W_g) of 3.2 mm. Fig. 6 shows the microphotograph of the fabricated PD MMIC, which has a size of 1.5×0.8 mm^2. $SrTiO_3$ capacitors were employed in order to reduce chip size compared with the use of SiN_x capacitors [24]. Fig. 7 shows the gain and phase deviations of the PD measured with a single-tone signal at 1.95 GHz as a function of V_c. Gain expansion and negative phase deviation are observed with increasing input power for V_c below -1.0 V. The degrees of gain expansion, phase deviation, and IL increase by reducing V_c. In handset application where power amplifiers operate slightly below the 1-dB compression point ($P_{1\ dB}$) [3], a 1-dB gain expansion from the PD would be sufficient for nonlinear gain compensation. Under such a condition, the PD achieves a low IL of less than 3.5 dB, which is significantly lower than other reported designs [13], [14]. Hence,

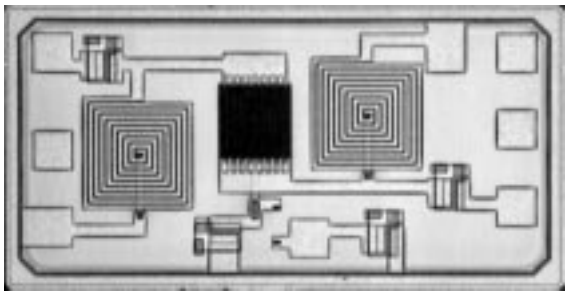


Fig. 6. Microphotograph of the PD MMIC based on an HJFET with a gatewidth of 3.2 mm (chip size 1.5×0.8 mm^2).

no extra buffer amplifier is required, and the low loss can be easily compensated by a driver amplifier before the power stage in handsets. Another interesting characteristic of the PD is that it

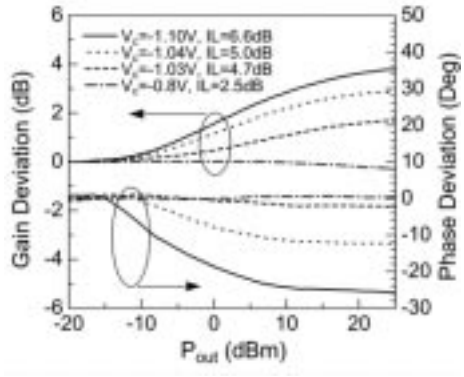


Fig. 7. Measured single-tone gain and phase deviations of the PD MMIC at 1.95 GHz as a function of the control voltage V_c.

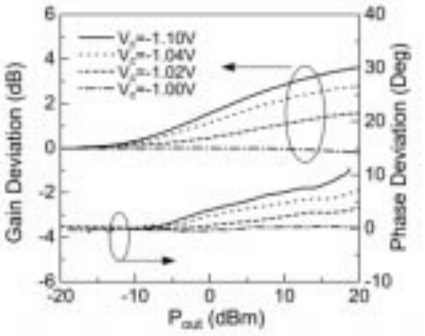


Fig. 8. Measured single-tone gain and phase deviations of the PD MMIC at 1.95 GHz without inductors L.

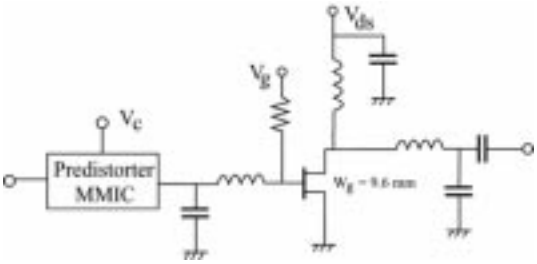


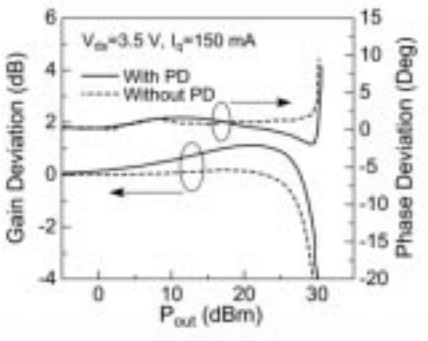
Fig. 9. Schematic of the linearized amplifier.

shows a slight gain compression for V_c above -1.0 V. This phenomenon is attributed to the increase in r_{ds} with input power.

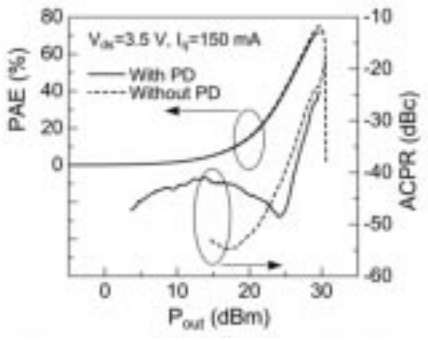
To verify the effect of inductors L on phase deviation, another PD was characterized with a similar structure to that in Fig. 6, but without L. Referring to Fig. 8, similar gain deviation is obtained as compared to the case with L. However, the PD shows an opposite phase characteristic, i.e., positive phase deviation, which agrees with the simulated results shown in Fig. 5.

IV. Power Performance of Linearized Amplifier

The schematic diagram of the linearized amplifier, incorporating the PD MMIC, is shown in Fig. 9. The amplifier is based on the double-doped HJFET discussed in Section II with a W_g of 9.6 mm. The input and output matching networks of the amplifier were designed and optimized to obtain the best PAE with an adjacent channel leakage power ratio (ACPR) equal to -40 dBc, measured at 1.95 GHz with an HPSK signal having a chip rate of



(a)



(b)

Fig. 10. Measured characteristics of the amplifier with and without PD at 1.95 GHz. (a) Single-tone gain and phase deviations. (b) ACPR and PAE using an HPSK signal. I_q was set equal to 150 mA. The PD was biased for gain expansion operation.

4.096 Mc/s. The performances of the linearized amplifier were evaluated under two different bias conditions; the first case was a high I_q operation at 150 mA (2.5% of I_{max}) and the second case was a low I_q operation at 45 mA (1% of I_{max}). The I_q was adjusted by varying the gate voltage (V_g) of the amplifier with the drain-to-source voltage (V_{ds}) set equal to 3.5 V.

A. High I_q Operation

Fig. 10(a) shows the gain and phase deviations of the linearized amplifier measured with a single-tone signal at 1.95 GHz for an I_q equal to 150 mA. V_c of the PD was adjusted to achieve a gain expansion characteristic. It can be seen that the $P_{1\,dB}$ of the amplifier is improved from 26.6 to 27.5 dBm after the use of the PD. Similarly, the linearized amplifier shows a lower phase deviation than the case without the PD. This demonstrates the effectiveness of the PD on linearizing the amplifier's nonlinear characteristics.

Fig. 10(b) shows the W-CDMA power performance of the linearized amplifier measured with the HPSK signal. The ACPR of the amplifier is reduced with the use of PD at an output power (P_{out}) above 23 dBm. The ACPR, however, is degraded below that power level due to the effect of gain expansion [see Fig. 10(a)], but it is below -40 dBc and, therefore, still satisfies the distortion requirement. Measured at -40 dBc ACPR, the P_{out} and PAE of the amplifier improve from 25.2 dBm and 43.0% to 26.2 dBm and 49.9%, respectively, after the use of the PD, attributed to a 5.4-dB reduction in ACPR after linearization. This represents an improvement on P_{out} and PAE by 1 dB and 6.9%, respectively.

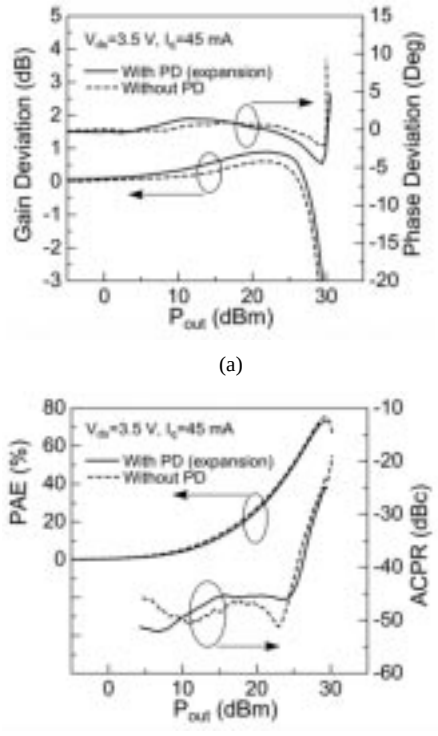


Fig. 11. Measured characteristics of the amplifier with and without the PD at 1.95 GHz. (a) Single-tone gain and phase deviations. (b) ACPR and PAE using an HPSK signal. $I_{\rm q}$ was set equal to 45 mA. The PD was biased for gain expansion operation.

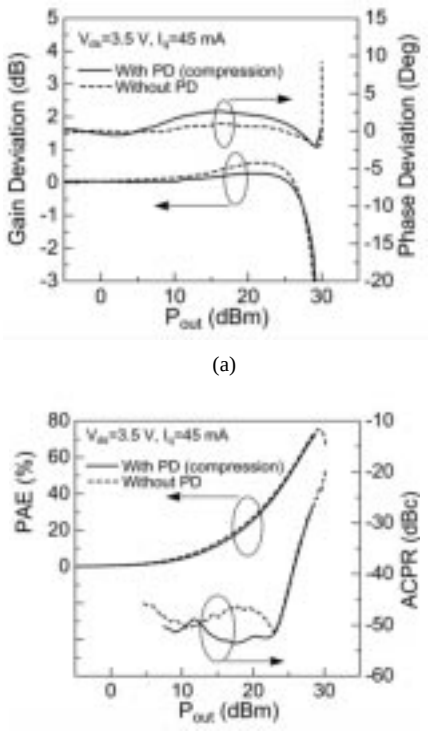


Fig. 12. Measured characteristics of the amplifier with and without the PD at 1.95 GHz. (a) Single-tone gain and phase deviations. (b) ACPR and PAE using an HPSK signal. $I_{\rm q}$ was set equal to 45 mA. The PD was biased for gain compression operation.

B. Low $I_{\rm q}$ Operation

We have previously shown that the HJFET amplifier under low $I_{\rm q}$ bias is favorable for high PAE operation under W-CDMA criteria [20]. This type of amplifier, however, experiences gain expansion with increasing $P_{\rm out}$ instead of the usual gain compression shown in the higher $I_{\rm q}$ case. Due to this, the use of the PD with two different responses was investigated; one with gain expansion and the other with slight gain compression. These two different characteristics were achieved by adjusting $V_{\rm c}$ of the PD shown in Fig. 9.

Fig. 11 shows the measured responses of the linearized amplifier with the use of a gain-expansion-type PD. The measured single-tone gain and phase deviations of the amplifier are depicted in Fig. 11(a). After linearization, the $P_{1\ \rm dB}$ of the amplifier improves from 27.7 to 28.3 dBm. The level of gain expansion at low $P_{\rm out}$ is further increased as a result of the response of PD. The linearized amplifier also shows a reduction in phase deviation. Fig. 11(b) shows the power performance of the linearized amplifier measured with the HPSK signal. The ACPR is degraded at low $P_{\rm out}$ due to the increased gain expansion by referring to Fig. 11(a). At $-$40-dBc ACPR, the PD with gain expansion improves the amplifier's $P_{\rm out}$ from 25.5 to 26.2 dBm and PAE from 54.4% to 57.4%, achieving a state-of-the-art performance for W-CDMA power amplifiers. The improvements result from a 5.0-dB decrease in ACPR after linearization.

The responses of the amplifier incorporating gain compression type PD are shown in Fig. 12. Referring to Fig. 12(a), the gain deviation of the linearized amplifier is reduced at $P_{\rm out}$ below 23 dBm, but the $P_{1\ \rm dB}$ of the amplifier is not improved due to the compression nature of the PD. The linearized amplifier, shown in Fig. 12(b), achieves significant ACPR reduction for $P_{\rm out}$ below 23 dBm, with a maximum improvement of 9.1 dB at 18 dBm $P_{\rm out}$ due to the flattened gain deviation. However, at the W-CDMA criteria, the linearized amplifier shows a similar performance to the case without the PD.

C. Discussion

Although the linearized amplifier operated under low $I_{\rm q}$ with the gain-expansion-type PD demonstrates the best PAE performance under W-CDMA criteria, the high $I_{\rm q}$ bias case achieves a more significant improvement on $P_{\rm out}$ and PAE (1 dB and 6.9%, respectively, compared to 0.7 dB and 3% for the low $I_{\rm q}$ case) despite having a similar degree of ACPR reduction. Since the basic principle of predistortion linearization is to give an amplifier a harder saturation characteristic, it is, therefore, more effective to compensate the softer compression shown in the high $I_{\rm q}$ case. Despite a lesser improvement under low $I_{\rm q}$ operation, the 5-dB decrease in ACPR and the 3% increase in PAE are still substantial for handset application. Due to the low-loss characteristic of the PD, the linearized amplifier, even as a one-stage design, does not require an extra buffer amplifier to bring up the signal level, as required in other reported designs [16]. This illustrates the linearized amplifier configuration can successfully achieve performance advancement without the penalties of additional components and power consumption.

Under high $I_{\rm q}$ operation, the choice of the response of the PD is straightforward. Since the amplifier experiences a gain compression characteristic, the PD is required to have an opposite

TABLE I
REQUIREMENTS ON THE PD FOR A GAIN-EXPANSION-TYPE AMPLIFIER (LOW I_q OPERATION)

Backoff level of amplifier	Requirements on predistorter
Near compression operation	Gain expansion type PD - to compensate gain compression (for moderate distortion improvement in application such as handsets)
High level power backoff operation	Gain compression type PD - to compensate gain expansion (for very low distortion amplification application such as basestation)

response, i.e., gain expansion. The increase in the ACPR at a low $P_{\rm out}$ level, shown in Fig. 10(b), is due to a slightly different onset of the gain compression of the amplifier and the gain expansion of the PD. Further improvement can be made by carefully optimizing the circuit parameters of the PD to match the response of the amplifier. On the contrary, the gain expansion characteristic of the amplifier under low I_q bias places a different requirement on the PD. The improvement on the ACPR can be divided into two operating regions: near compression and high power backoff operation. When the amplifier is operated near compression point, such as in handset application [3], the gain-expansion-type PD is required to bring up $P_{1\ \rm dB}$ of the amplifier, as shown in Fig. 11, for ACPR and PAE improvements. This comes at the expenses of increasing low $P_{\rm out}$ gain deviation, resulting in a degraded ACPR. On the other hand, when very low-distortion amplification is required, such as in basestation application, high-power backoff from saturation power is usually required even with the use of linearization technique [8]. Under such a condition, the PD with a gain compression response is applicable for reducing the distortion level of amplifiers (see Fig. 12). Table I summarizes the PD requirements on a gain-expansion-type amplifier (low I_q bias). In application where low distortion over a wide range of $P_{\rm out}$ is needed, intelligent bias control can be applied to the PD, such that V_c is adjusted automatically according to the $P_{\rm out}$ level.

V. LINEARIZED AMPLIFIER WITH BIAS CONTROL

With the implementation of a power control scheme in the W-CDMA system, a low $P_{\rm out}$ characteristic of handset amplifiers is also an important design concern [2]. Although the linearized amplifier, operated at low I_q and employing a gain-expansion-type PD, as shown in Fig. 11, demonstrates the best PAE characteristic, the performance degrades significantly when $P_{\rm out}$ is reduced, attaining only 8.0% PAE at 13 dBm $P_{\rm out}$. This would have an adverse effect on battery life in handsets, resulting in shorter talk time. Bias control has been reported as an attractive alternative for improving PAE at low $P_{\rm out}$ operation [20], [25]. By lowering the supply current and voltage of an amplifier, the saturation power reduces and, therefore, improves PAE at a low $P_{\rm out}$ region since less backoff is required.

The incorporation of bias control together with predistortion linearization for further improving PAE of the amplifier at low $P_{\rm out}$ was investigated. Referring to Fig. 9, the bias control was

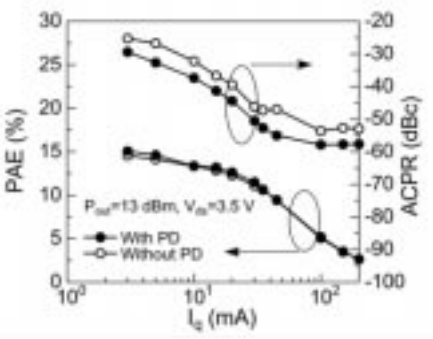


Fig. 13. Measured PAE and ACPR of the amplifier with and without the PD at 13 dBm $P_{\rm out}$. Bias control was applied on I_q.

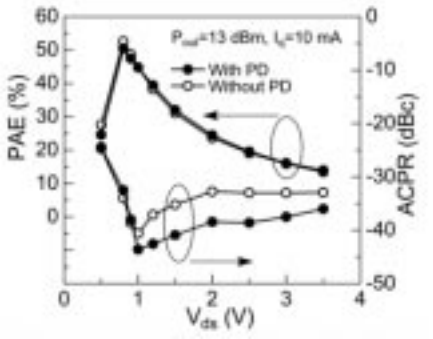


Fig. 14. Measured PAE and ACPR of the amplifier with and without the PD at 13 dBm $P_{\rm out}$. Bias control was applied on $V_{\rm ds}$.

obtained by varying I_q (by means of V_g) and $V_{\rm ds}$ of the amplifier. Fig. 13 illustrates the dependence of PAE and the ACPR of the amplifier (with and without the PD) on I_q at a constant $P_{\rm out}$ of 13 dBm. It can be seen that the PAE increases by reducing I_q, but this degrades the ACPR. With the use of the PD, however, ACPR reduction is achieved, allowing the amplifier to operate at a lower I_q level to further improve the PAE. At 13-dBm $P_{\rm out}$ and -40-dBc ACPR, the linearized amplifier shows a PAE of 13.6% at I_q of 10 mA, which is 5.6% higher than the case without bias control.

Fig. 14 shows similar measured results, but as a function of $V_{\rm ds}$ at a constant I_q of 10 mA. The PAE improves more significantly when compared to that of I_q control (Fig. 13), showing a PAE of 47.7% at the same output criteria. This represents an improvement of almost sixfold after implementing bias control. The APCR is also reduced with the use of the PD in this case. However, at $V_{\rm ds}$ below 0.9 V, the ACPR increases sharply as the amplifier operates at a deep saturation power level at which the PD cannot provide further distortion improvement.

Fig. 15 compares the PAE of the amplifier with and without the PD and bias control over a range of $P_{\rm out}$ from 0 to 26 dBm. The best PAE is achieved by simultaneously controlling $V_{\rm ds}$, I_q and V_c. The linearized amplifier shows a PAE of over 40% for a 20-dB $P_{\rm out}$ range, which would be sufficient for W-CDMA application. This performance is attributed to two factors: first is the use of the PD, which reduces the ACPR at the amplifier output, allowing it to operate at less power backoff, and second is the realization of bias control, which improves low $P_{\rm out}$ characteristic. These results demonstrate that PD can be employed for improving PAE at both the low and high $P_{\rm out}$ level.

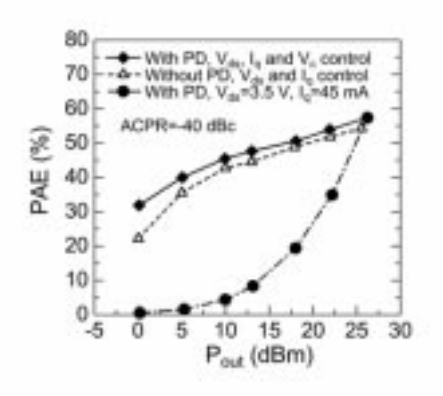


Fig. 15. Comparison of PAE of the amplifier with and without the PD using $V_{\rm ds}$, $I_{\rm q}$, and $V_{\rm c}$ control at -40-dBc ACPR.

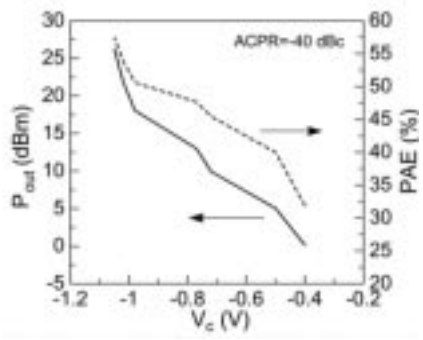


Fig. 16. Dependence of $P_{\rm out}$ and PAE of the linearized amplifier on control voltage ($V_{\rm c}$) of the PD with bias control at -40-dBc ACPR.

The control on $V_{\rm c}$ of the PD plays a critical part in obtaining the performance improvement discussed above. Fig. 16 depicts the $P_{\rm out}$ and PAE of the linearized amplifier as a function of $V_{\rm c}$. $V_{\rm ds}$, $I_{\rm q}$, and $V_{\rm c}$ were adjusted accordingly to obtain the best PAE at each measured $P_{\rm out}$ point over the range from 0 to 26 dBm for -40-dBc ACPR. It is observed that the required $V_{\rm c}$ varies linearly with $P_{\rm out}$ and PAE. This linear characteristic is an added advantage and can reduce the complexity when implementing intelligent control on the PD.

VI. Conclusions

Modern digital wireless systems demand high-linearity high-efficiency amplifiers for handset application. Predistortion linearization has been shown to be an effective technique, in terms of simple configuration and compact size, for compensating amplifier nonlinearities and enhancing performances. A low-loss PD MMIC has been presented, achieving gain expansion and compression characteristics depending on the control voltage. The requirement on the characteristic of the PD due to the variation of amplifier's response under high and low $I_{\rm q}$ operations has been detailed. In both cases, the PD effectively linearizes the amplifier's nonlinearities and reduces output distortion, allowing the amplifier to operate at less powerful backoff and, thus, improving the PAE. Under a low $I_{\rm q}$ operation, PAE of 57.4% has been obtained on the amplifier with the PD under W-CDMA criteria. The PD has been demonstrated to perform well in terms of linearizing the amplifier over a wide range of output power. Combining with a bias control scheme, PAE of over 40% has been achieved on the linearized amplifier over a 20-dB output power range. Such a characteristic is desirable for application in wireless systems, such as W-CDMA, which implement power control.

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